Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently amended): A vertical dynamic random access memory (DRAM) comprising:

a substrate comprising at least a deep trench having an upper trench portion and a lower trench portion;

a trench capacitor located in the lower trench portion;

a source-isolation oxide layer located on the trench capacitor;

a shallow trench isolation (STI) positioned around the deep trench; and

a vertical transistor located on the source-isolation oxide layer, the vertical transistor comprising:

an annular source set in the substrate next to the source-isolation oxide layer, the annular source being electrically connected to the trench capacitor;

a gate conductive layer filling the upper trench portion and electrically connected to a first contact plug;

a cylindrical gate dielectric layer located on a surface of a sidewall of the upper trench portion and circularly encompassing the gate conductive layer; and

an annular drain circularly encompassing the deep trench near a surface of the substrate, the annular drain being positioned next to the STI and electrically connected to a second contact plug, the STI completely compassing the vertical transistor and separating the annular drain from other annular drains of any adjacent vertical transistors in the substrate. ~~and being isolated from the annular drains of adjacent vertical transistors by the STI.~~

Claim 2 (original): The vertical DRAM of claim 1, wherein the trench capacitor

comprises:

a storage node filling the lower trench portion and electrically connected to the annular source;

a capacitor dielectric layer encompassing the storage node; and

a buried plate located in the substrate in a side of the capacitor dielectric layer.

Claim 3 (original): The vertical DRAM of claim 2, wherein the buried plate surrounds a sidewall of the lower trench portion, and the capacitor dielectric layer is located on a surface of the sidewall of the lower trench portion so as to isolate the storage node and the buried plate.

Claim 4 (original): The vertical DRAM of claim 2, wherein the trench capacitor further comprises a buried strap for electrically connecting the annular source and the storage node.

Claim 5 (Previously presented): The vertical DRAM of claim 4, wherein the buried strap is an annular conductive strap located on the inner surface of the sidewall of the lower trench portion above the capacitor dielectric layer.

Claim 6 (original): The vertical DRAM of claim 1, wherein the vertical DRAM further comprises a conductive layer located on the gate conductive layer for electrically connecting the gate conductive layer and the first contact plug.

Claim 7 (original): The vertical DRAM of claim 1, wherein the annular source is an ion diffusion area.

Claim 8 (original): The vertical DRAM of claim 1, wherein the annular drain overlaps a heavily doped ion implantation area.

Claim 9 (original): The vertical DRAM of claim 1, wherein the vertical DRAM further comprises a passivation layer covering the surface of the substrate and the transistor.

Claim 10 (original): The vertical DRAM of claim 1, wherein the first and the second contact plug are electrically connected to a word line and a bit line respectively.

Claim 11 (Previously presented): The vertical DRAM of claim 1, wherein the shallow trench isolation surrounds the annular source and the annular drain without overlapping the deep trench.

Claim 12 (currently amended): The vertical DRAM of claim 1, wherein the vertical DRAM further comprises an annular spacer surrounding the entire upper trench portion.

Claim 13 (Currently amended): The vertical DRAM of claim 12, wherein the second contact plug has an asymmetric structure, which is positioned on the annular spacer and the annular drain while contacts the spacer and the annular drain at the same time.

Claim 14 (New): The vertical DRAM of claim 13, wherein the second contact plug further contacts the STI at a first side of the second contact plug while contacts the annular spacer at a second side of the second contact plug, the second side being opposite to the first side of the second contact plug.

Claim 15 (New): The vertical DRAM of claim 12, wherein the annular spacer positioned on an outer surface of the sidewall of the entire upper trench portion.

Claim 16 (New): The vertical DRAM of claim 1, wherein the annular drain around the sidewall of the deep trench has an asymmetric structure, a portion of the annular drain positioned below the second contact plug having a larger width from the STI to the deep trench than a width of a portion of the annular drain not positioned below the second contact plug.

Claim 17 (New): A method for fabricating a vertical DRAM, the method comprising:

providing a substrate having a pad layer thereon and a trench capacitor formed in

a deep trench, the trench capacitor comprising a storage node in the deep trench, a capacitor dielectric layer on a sidewall of the deep trench, and a buried plate in the substrate around the deep trench;

forming a first doped silicate layer on the storage node and the capacitor dielectric layer;

performing a diffusion process to form a first annular ion diffusion area serving as an annular source in the substrate near the first doped silicate layer;

removing a portion of the first doped silicate layer which is on the storage node, and leaving the other portion of the first doped silicate layer that is positioned on the capacitor dielectric layer and on an inner surface of the sidewall of the deep trench, wherein the remaining first doped silicate layer serves as a buried strap;

forming a source-isolation oxide layer in the deep trench and positioned on the storage node, the capacitor dielectric layer, and the buried strap;

forming a gate dielectric layer on the inner surface of the sidewall of the deep trench, positioned on the source-isolation oxide layer;

forming a first doped polysilicon layer on the source-isolation oxide layer and filling the deep trench, the first doped polysilicon layer serving as a gate;

forming a second doped silicate layer on the first doped polysilicon layer and performing a diffusion process to form a second annular ion diffusion area around the deep trench in the substrate, the second annular ion diffusion area serving as an annular drain;

removing the second doped silicate layer;

depositing an oxide layer and a nitride layer on the substrate sequentially;

etching back the nitride layer and the oxide layer to form a spacer on the inner surface of the sidewall of the deep trench and expose a portion of the first doped polysilicon layer;

forming a second doped polysilicon layer on the exposed first doped polysilicon layer;

forming a shallow trench isolation (STI) in the substrate around the deep trench, the first and the second annular ion diffusion area, a first distance between a first side of the deep trench and the STI is larger than a second distance

between a second side of the deep trench and the STI;

etching the pad layer; and

performing an ion implanting process to form a heavily doped ion implantation area overlapping a portion of the second annular ion diffusion area, which is at the first side of the deep trench.

Claim 18 (New): The method of claim 17, wherein the first doped silicate layer and/or the second doped silicate layer are formed by arsenic silicate glass (ASG).

Claim 19 (New): The method of claim 17, wherein the annular source is positioned next to the buried strap, the source-isolation oxide layer, and a bottom of the gate dielectric layer.

Claim 20 (New): The method of claim 17, wherein the step of forming the gate dielectric layer comprises performing an oxidization process to oxidize the sidewall of the deep trench.

Claim 21 (New): The method of claim 17, wherein the method further comprises performing a recess etching (RE) process after forming the first doped polysilicon layer to make a surface of the first doped polysilicon layer lower than a surface of the substrate.

Claim 22 (New): The method of claim 17, wherein the method further comprises performing a chemical mechanical polishing (CMP) process before forming the STI, so that a surface of the second doped polysilicon layer is approximately coplanar with a surface of the pad alyer.

Claim 23 (New): The method of claim 17, wherein the method further comprises:

forming a passivation layer and an inter layer dielectric (ILD) layer on the substrate sequentially; and

forming a first contact plug positioned on and electrically connecting to the second doped polysilicon layer, and a second contact plug positioned on and

electrically connecting to the heavily doped ion implantation area.

Claim 24 (New): The method of claim 23, wherein the step of forming the first and the second contact plugs compries:

performing a photolithography and etching process (PEP) to define a first contact hole and a second contact hole which expose the second doped silicon layer and the heavily doped ion implantation area respectively;

depositing a conductive layer on the substrate, wherein the conductive layer fills the first and the second contact holes; and

performing a CMP process to remove a portion of the conductive layer positioned above the ILD layer.

Claim 25 (New): The method of claim 24, wherein the conductive layer is formed by a material selected from the group consisting of metal or doped polysilicon.

Claim 26 (New): The method of claim 23, wherein the method further comprises forming a word line and a bit line on the substrate, the word line and the bit line electrically connecting to the first contact plug and the second contact plug respectively.

Claim 27 (New): The method of claim 23, wherein the annular drain has an asymmetric structure, a portion of the annular drain positioned below the second contact plug having a larger width from the STI to the deep trench than a width of a portion of the annular drain not positioned below the second contact plug.

Claim 28 (New): The method of claim 23, wherein the second contact plug has an asymmetric structure, which is positioned on the annular drain and the STI while contacts the annular drain and the STI at the same time.

Claim 29 (New): The method of claim 17, wherein an annular spacer is formed on an outer surface of the oxide layer and surrounding the deep trench after etching the pad

layer.